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a cylindrical hole extending through said first conductive film below said second opening, said first conductive film is etched until said insulating interlayer is exposed in said first opening;

the ninth step of forming a dielectric film so as to cover a surface of said first conductive film; and

the tenth step of forming a second conductive film so as to cover said dielectric film opposing said first conductive film through said dielectric film.

REMARKS

Claims 28-36, 38-42, 44, and 45 are presently pending in the application. Claims 28-31 are allowed. Favorable reconsideration of the rejected claims is requested.

Entry of the amendment to claim 32 is requested in order to make it clear that the subject matter of claim 32 conforms to the embodiments disclosed in Figs. 10A-10K, 12A-12E, and 14A-14E.

Withdrawal of the objection to the specification concerning the subject matter of claim 32 is requested. It is submitted that the foregoing amendments to claim 32 will make it clear that the sixth step of etching divides the conductive film at a location above the isolation structure. This will be fully supported by the subject matter of Figs. 10A-10K. Withdrawal of the rejection of claims 32-35 under 35 U.S.C. § 112, is requested in light of the proposed amendment.

Withdrawal of the rejection of claims 42, 44, and 45 under 35 U.S.C. § 112, is respectfully requested in light of the amendments made hereto.

Withdrawal of the rejection of claims 36 and 42 under 35 U.S.C. § 102(e) as being anticipated by Schoenfeld et al. (U.S. Pat. No. 6,010,932) is requested. Claim 42 describes a multi-step process which includes performing a insulating interlayer in step four which serves as a stopper. When the hole 54 is formed in the conductive layer, it exposes, as shown in Fig. 12B, the insulating layer while simultaneously forming a second hole 49 through the first conductive film of Fig. 10I-12B. The cylindrical hole 54 in the conductive film extending below the second opening permits for a increase in capacitance. In reviewing the Schoenfeld et al. reference, there is no cylindrical opening in the conductor described. In reviewing Schoenfeld et al., recesses 144 are shown in the conductive film which do not extend all the way through to the insulating layer, nor do they appear to form any cylindrical opening in the conductor.

Withdrawal of the rejection of claims 38 and 39 as being unpatentable over Komori et al. (U.S. Pat. No. 5,300,802) in view of Wolf et al. (Vol. 1) is requested. As noted in the Office Action, Komori et al does not disclose the patterning of the first conductive layer so that the conductive film is divided below a first opening and extends below a second opening formed in the conductive film.

Turning now to the secondary reference of Wolf et al., it is not seen, how as set forth in claim 36, any element isolation structure would be exposed in creating the first and second openings by using the element isolation structure as a stopper. As set forth in rejected claim 38, the first conductive film is divided below the first opening while a hole is simultaneously made as a second opening which is also undisclosed in Wolf et al.

Unless this structure can be found in the cited references, no combination of the references would yield or suggest the subject matter.

As claim 39 is dependent on claim 38, it is considered to be allowable as well.

Claims 40-41, are dependent on claim 38 and otherwise believed to be allowable.

Withdrawal of the rejection of claim 44 is requested. Claim 44 is dependent on claim 2 and carries all of the limitations thereof.

Withdrawal of the rejection of claims 44 and 45 is requested. Claims 44 and 45 are dependent on claim 42 and carry all of the limitations thereof.

In view of the foregoing, wherein amendments have been made to make clear that the current subject matter is not suggested in the prior art, favorable reconsideration is requested.

The Director is hereby authorized to charge any fees, or credit any overpayment, associated with this communication, including any extension fees, to CBLH Deposit Account No. 22-0185.

Respectfully submitted,

By _____

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MARKED-UP REVISIONS

IN THE CLAIMS:

Kindly amend the claims as follows:

32. (Amended) A method of fabricating a semiconductor device, comprising:

the first step of defining an element active region by forming an element isolation structure on a semiconductor substrate;

the second step of forming a gate insulating film and a gate electrode in said element active region;

the third step of doping an impurity into said active region of said substrate to form a pair of impurity diffusion layers in surface regions of said semiconductor substrate on two sides of said gate electrode;

the fourth step of forming a first conductive film electrically connected to one of said impurity diffusion layers;

the fifth step of forming a mask pattern having at least first and second openings on said first conductive film;

the sixth step of etching said first conductive film by using said mask pattern as a mask until said first opening [extends to said element isolation structure, thereby dividing] divides said first conductive film in said first opening above said isolation structure, and simultaneously [forming] forms a recess in said second opening having said first conductive film forming a bottom of said recess;

the seventh step of forming a dielectric film so as to cover a surface of said first conductive film; and

the eighth step of forming a second conductive film on said dielectric film opposing said first conductive film through said dielectric film.

42. (Amended) A method of fabricating a semiconductor substrate, comprising:

the first step of defining an element active region by forming an element isolation structure on a semiconductor substrate;

the second step of forming a gate oxide film and a gate electrode on said semiconductor substrate in said element active region;

the third step of doping an impurity into said semiconductor substrate in said element active region to form a pair of impurity diffusion layers in surface regions of said semiconductor substrate on two sides of said gate electrode;

the fourth step of forming an insulating interlayer on an entire surface of said semiconductor substrate;

the fifth step of forming a hole in said insulating interlayer in which one of said impurity diffusion layers is exposed;

the sixth step of forming a first conductive film on said insulating interlayer which fills said hole electrically connected to one of said impurity diffusion layers [covering];

the seventh step of forming a mask pattern having at least first and second openings on said first conductive film;

the eighth step of etching said first conductive film by using said mask pattern as a mask, thereby dividing said first conductive film below said first opening, and simultaneously forming a cylindrical hole extending through said first conductive film below said second opening, said first conductive film is etched until said insulating interlayer is exposed in said first opening;

the ninth step of forming a dielectric film so as to cover a surface of said first conductive film; and

the tenth step of forming a second conductive film so as to cover said dielectric film opposing said first conductive film through said dielectric film.